Notice of Allowability	Application No.	Applicant(s)	
	09/955,131	YABE, TOMOAKI	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on February 28, 2005*.

2. ☒ The allowed claim(s) is/are *4 -11 and 15 - 20, renumbered 1 - 8 and 9 - 14, respectively*.

3. ☒ The drawings filed on *19 September 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gary D. Fedoeochko on 04/08/2005.

The application has been amended as follows:

Claim 4 rewrite as: A phase detector configured to output an up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, said phase detector comprising: first, second, and third flip-flops; a flip-flop (F/F) control circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flop are in set state, brings said third flip-flop to the set state when said second clock signal has a second logic ad said first flip-flop is in reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and an up-down signal output circuit configured to output said up signal and down signal based on the outputs of said second and third flip-flops.

Claim 5 rewrite as: The phase detector according to claim 4 wherein said flip-flop (F/F) control circuit comprises: a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic; a second logic circuit configured t bring said second flip-flop to the set state when said flip-flop is in the reset state and said first clock signal had said second logic; a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic; a fourth logic circuit configured to bring said second and third flip-flop to the reset state when said second and third flip-flops are in the set state; a fifth logic circuit configured to output an up signal when said second flip-flop is in the set state and third flip-flop is in the reset state; and a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Claim 15 rewrite as: A phase locked loop circuit comprising: a charge pump configured to output a voltage signal in accordance with an up signal and a down signal; a loop filter configured to remove a high frequency component included in the an output of said charge pump; a voltage control oscillation circuit configured to output a signal of a frequency in accordance with output voltage of said loop filter; a clock buffer configured to output a clock signal in accordance with an output of said voltage control oscillation circuit; and a phase detector configured to output the up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, wherein said phase detector comprises: first, second, and third flip-flops; a flip-flop (F/F) control

circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flop are in set state, brings said third flip-flop to the set state when said second clock signal has a second logic ad said first flip-flop is in reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and an up-down signal output circuit configured to output said up signal and down signal based on the outputs of said second and third flip-flops.

Claim 16 rewrite as: The phase locked loop circuit according to claim 4 wherein said flip-flop (F/F) control circuit comprises: a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic; a second logic circuit configured t bring said second flip-flop to the set state when said flip-flop is in the reset state and said first clock signal had said second logic; a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic; a fourth logic circuit configured to bring said second and third flip-flop to the reset state when said second and third flip-flops are in the set state; a fifth logic circuit configured to output an up signal when said second flip-flop is in the set state and third flip-flop is in the reset state; and a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Reason For Allowance

The following is an examiner's statement of reasons for allowance: Prior art of record failed to teach phase detector comprising: first, second, and third flip-flops; a flip-flop (F/F) control circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flop are in set state, brings said third flip-flop to the set state when said second clock signal has a second logic ad said first flip-flop is in reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and an up-down signal output circuit configured to output said up signal and down signal based on the outputs of said second and third flip-flops..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
04/11/2005

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600